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Using Statistical Methods to Validate Hardware Performance Monitors

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HPC-ENV
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What are Hardware Performance Monitors?

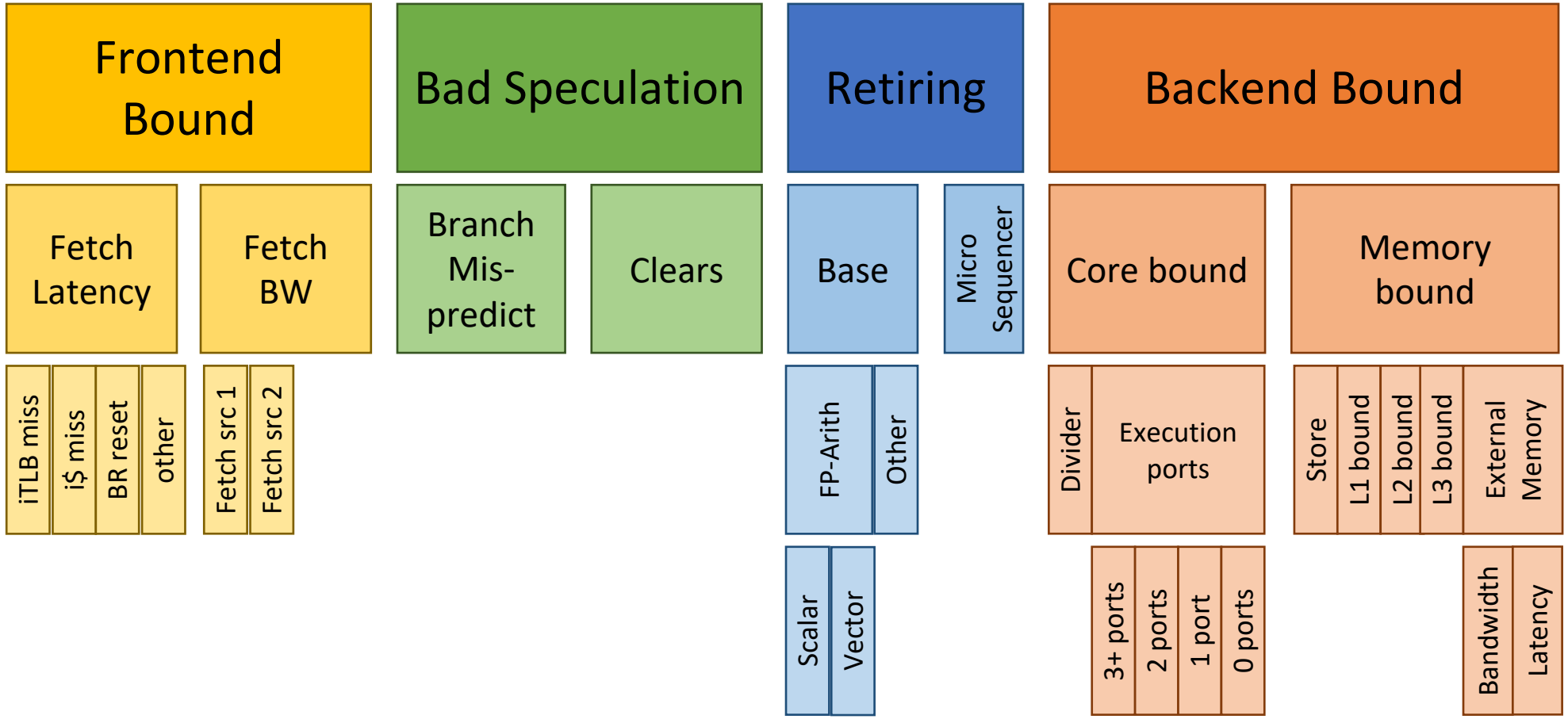
- HPMs are used for performance analysis
  - Hardware Counters
  - Bridge the gap between application and hardware
  - Cover numerous features of the hardware
  - Count events that occur while an application runs

How are they used?

- Many ways
- Usually ad hoc
- Specific issues are investigated
  - IPC
  - Cache miss rates
  - FLOP counts
  - Memory Bandwidth

Top-Down Method

- An alternative organized method for using HPMs



Top-Down Method

- Top Down was designed for Intel XEON Systems
- But there are many other vendors
- Systems of interest
  - AMD Rome
  - ARM/Marvell Thunder
  - ARM/Fujitsu A64FX

- Will Top Down work?

Portability of HPMs

- Portability of applications is increasingly important
  - Consistent metrics across systems would help
- Challenges
  - Vendors have different counter designs
  - Different system architectures
  - Inconsistent correctness

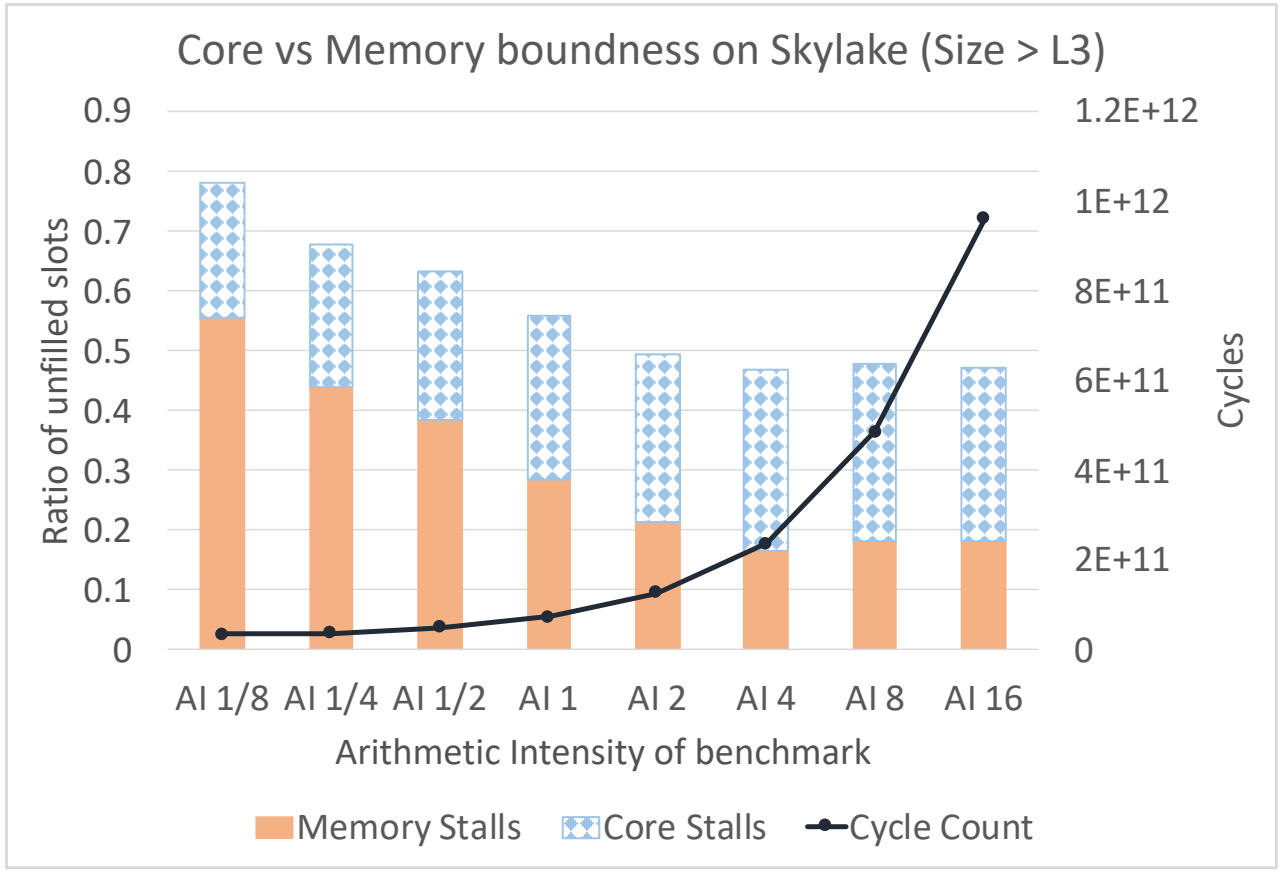
Solutions

- Benchmarks with known problems
  - These must be problems common to all or most systems
  - Verify the counters used to identify problems

- These benchmarks provide two things
  - Common language for developers to use across systems
  - Methods to validate measurements

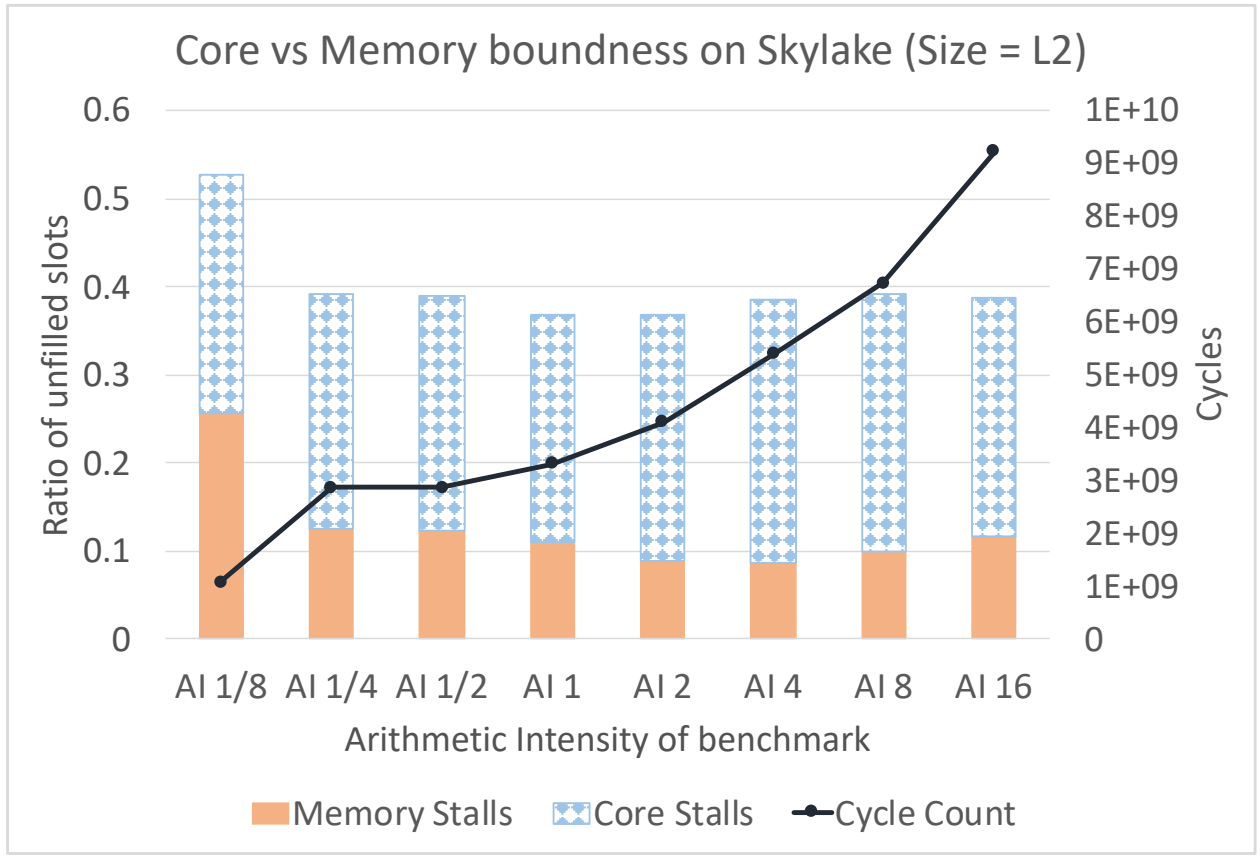
Benchmark

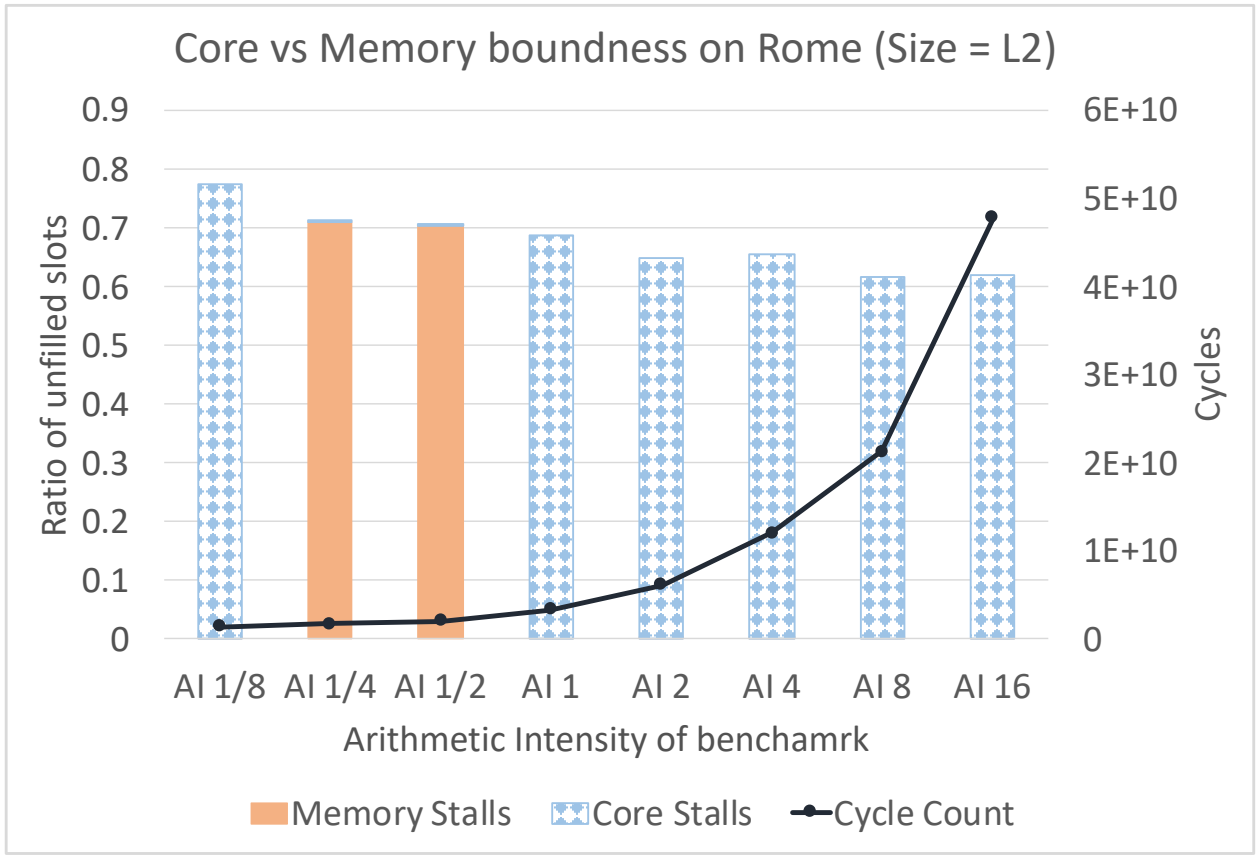
```
for elem in array
   load element
   sum = 0
   for FLOPS per load
      sum += elem
   store sum to elem
```



Results

- Educated guessing of counters was unsuccessful





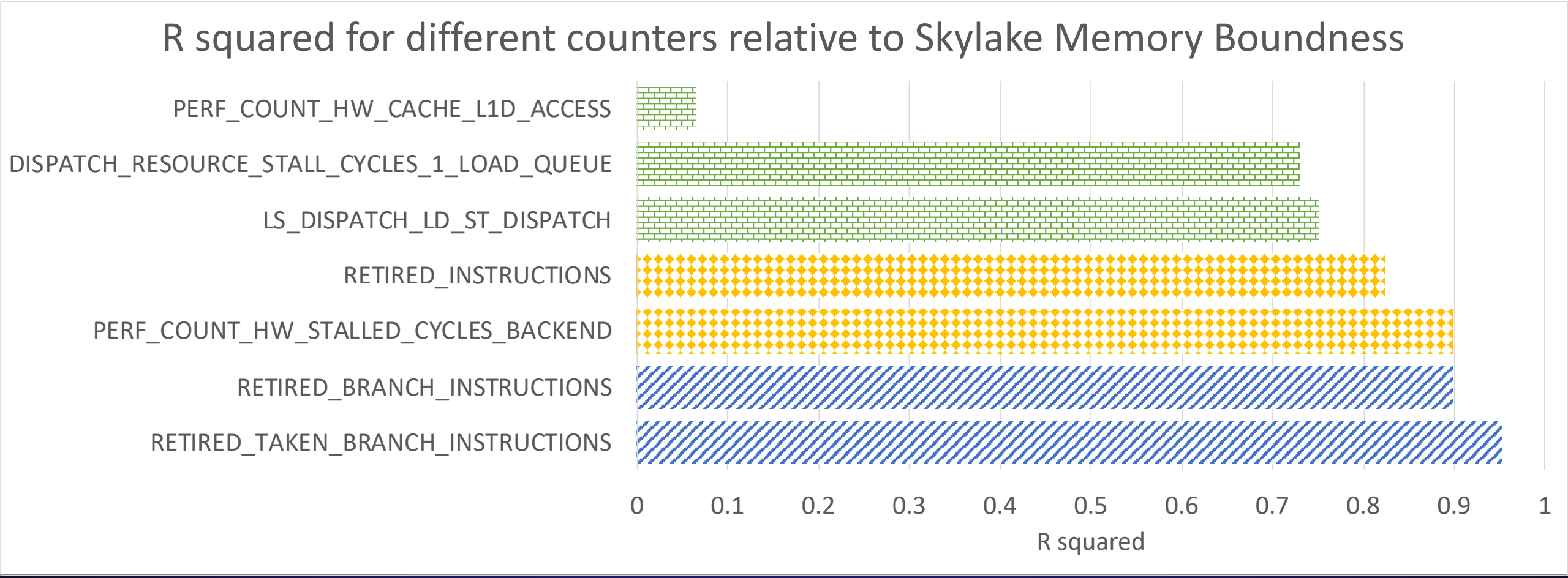
Results

- How do we find the counters we need?

- Why not try them all?
  - About 50 to 60 of interest on Rome
  - Compare results to the Skylake Memory boundness
  - Linear Regression

Results

- Linear regression to test all of the counters



Future Work

- Improve benchmark and fitting
- Add benchmarks for other performance issues
- Explore other architectures
- Apply to real application

Questions?

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