Brian Gravelle
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Using Statistical Methods to Validate Hardware Performance Monitors

High Performance Computing has benefited from rapid increases in the performance of processor architecture, but many applications must be updated to take advantage of new features. Hardware Performance counters are commonly used to examine how an application is using a particular system. Unfortunately, these HPMs differ significantly between processor vendors and generations. These differences inhibit developers trying to study performance on multiple systems, or trying to understand performance on a new system. In this talk, we present preliminary results defining and validating counter sets that expose performance metrics common to all modern HPC CPUs. These counters sets will help improve the portability of performance analysis. We present our novel benchmark for identifying counters of interest and results on multiple types of HPC nodes.